REMARKS

Status of the Claims

Claims 1, 5-9 and 12-26 are now present in this application. Claims 1, 12, 19 and 21 are independent.

By this Amendment, claims 24-26 are added, and claims 1, 12, 19 and 21 have been amended. Support for the new claims is found in the application as originally filed, including in paragraph [0047].

Reconsideration of this application, as amended, is respectfully requested.

Examiner Interview

Applicant wishes to thank Examiners Lauren Nguyen and David Nelms for the courtesies extended to Applicant's representative, Robert J. Webster, Reg. No. 46,472, during the personal interview which was conducted on January 4, 2010. The patentability of the existing claims and of possible proposed changes to the claims were discussed in an attempt to overcome the prior art rejections of record. The claims have been amended in the manner discussed during the interview, and are believed to place the application into condition for allowance. Accordingly, reconsideration and allowance of the present application are respectfully requested.

Rejection Under 35 U.S.C. § 102

Claims 21 and 22 stand rejected under 35 U.S.C. § 102(b) as being unpatentable over U.S. Patent 6,052,171 to Kawaguchi. This rejection is respectfully traversed.

Claim 21, as amended, recites a line-on glass liquid crystal display panel having sides and corners defined at intersections of the sides, comprising: a picture display part with a matrix of liquid crystal cells having a plurality of gate lines and data lines to cross each other; a gate pad and a data pad to drive the gate lines and data lines, respectively, the gate pad and the data pad are formed in an outer area of the picture display part of a low substrate on respective intersecting sides which define one corner; a plurality of line-on glass type signal lines located in one corner of the outer area of the picture display part of the lower substrate extending from one side to the other intersecting side that defines the one corner for applying drive gate signals to drive the liquid crystal cells, wherein the plurality of line-on-glass signal lines are located

between the gate pad and the data pad; and a common voltage line located in the one corner, wherein the common voltage line is adjacent to both the gate pad and the data pad.

Claim 22 depends from claim 21 and further recites that the gate signal lines are Vgl, Vcc, Vgh, GOE, GSC, GSP.

Kawaguchi clearly does not disclose these claimed combinations of features, including, for example, a plurality of line-on glass type signal lines located in one corner of the outer area of the picture display part of the lower substrate extending from one side to the other intersecting side that defines the one corner for applying drive gate signals to drive the liquid crystal cells, wherein the plurality of line-on-glass signal lines are located between the gate pad and the data pad.

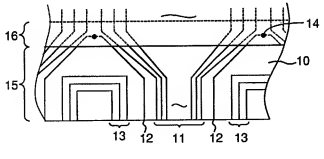
Accordingly, reconsideration and withdrawal of this rejection are respectfully requested.

Rejections under 35 U.S.C. § 103(a)

Claims 1-3, 5-6, and 12-16 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kawaguchi, US 6,052,171 (hereinafter "Kawaguchi") in view of Kim et al., KR 10-1999-0024956 (hereinafter "Kim"). Claims 19-20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kawaguchi in view of Kim and further in view of Song et al., US 2002/0008794 (hereinafter "Song"). Claim 23 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Kawaguchi in view of Song. These rejections are respectfully traversed.

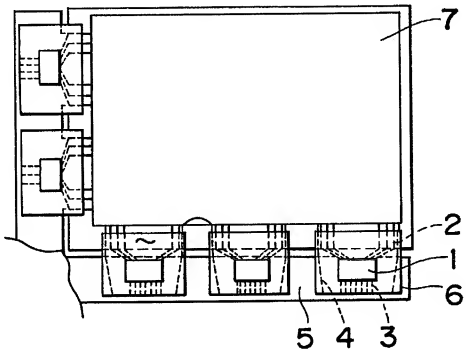
In Fig. 1A of Kawaguchi, the peripheral part 15 is one side of liquid crystal panel 10. That is, the peripheral part 15 corresponds to source line 11 and an upper side or a lower side of quadrilateral liquid crystal panel 10.

Fig.1A



Figs. 1A-1C of Kawaguchi show the TCP and its connection with liquid crystal panel 10 and circuit board 30. The TCPs 6 are formed in the lower side of the liquid crystal panel 10, not in one corner between the first gate pad and the first data pad. Please see Fig. 5 of Kawaguchi. Therefore, the shown peripheral part of Fig. 1A is just one side of the liquid crystal panel 10.

Fig.5 PRIOR ART



In column 6, lines 60-65, Kawaguchi also mentions that the embodiment is applicable to the gate line side, and similar effects can be obtained.

Herein, the gate line side corresponds to the left side or right side of the liquid crystal panel 10, not the one corner between the first gate pad and the first data pad. Thus, Kawaguchi does not teach or suggest a plurality of first line-on glass signal pads formed just beside the first data pad and a plurality of second line-on glass signal pads formed just beside the first gate pad, the first and second line-on glass signals pads are on respective intersecting sides which define one corner of the outer area of the picture display part; a plurality of line-on glass type signal lines connecting the first and second line-on glass signal pads in the corner of the outer area of the picture display part for applying gate power voltage signals and gate control signals to gate

drive ICs in order to drive gate signal lines of the picture display part; a plurality of first dummy pads between the first line-on glass type signal pads and a plurality of second dummy pads between the second line-on glass type signal pads; and a plurality of dummy lines connecting the first and second dummy pads in the one corner of the outer area of the picture display part, wherein the plurality of first and second dummy lines are formed between the line-on glass type signal lines for applying a common voltage as a reference voltage to drive the liquid crystal cells with at least one layer of insulating film therebetween, wherein the insulating film covers the plurality of line-on glass type signal lines and the dummy lines are formed on the layer of insulating film.

Moreover, Kawaguchi does not show any LOG type lines or LOG pads. LOG type lines are used to omit gate PCBs. In this case, the present invention discloses that LOG lines and LOG pads are formed in one corner between the first gate pad and the first data pad, and the LOG pads are connected to the first data TCP and the first gate TCP. That is, the gate control signals are directly received from the data PCB through the first data TCP without the gate PCB. However, Kawaguchi is regarding TCP type bonding. In this case, Kawaguchi calls for both the gate PCB and the source (data) PCB to be connected to respective gate and source TCPs.

Also, Kim and Song fail to disclose the above features. Accordingly, none of the cited references, including Kawaguchi, Kim and Song, teach the above features. Accordingly, claim 1 is considered allowable over Kawaguchi, Kim and Song, and claims 5-6, which depend from claim 1, are also considered to be allowable over the cited references.

Moreover, claim 12 is additionally allowable over Kawaguchi and Kim in that claim 12 recites the following features:

"forming first~ (n)th gate lines in a picture display part and a plurality of line-on glass signal lines in one corner of an outer area of the picture display part on a substrate for applying gate power voltage signals and gate control signals to gate drive ICs in order to drive gate signal lines of the picture display part;

forming at least one layer of insulating film to cover the line-on glass type signal lines; forming first~(m)th data lines to cross the first~ (n)th gate lines in a picture display part and a dummy line that is located between the line-on glass signal lines on the insulating film for applying a common voltage as a reference voltage; and

forming first~(m)th data pads extended from the first~(m)th data lines and first~ (n)th

gate pads extended from the first~(n)th gate lines in the outer of the picture display part and forming first and second line-on glass signal pads just beside the first data pad and first gate pad, respectively and first dummy pads between the first line-on glass signal pads and second dummy pads between the second line-on glass pads, respectively, in one corner of the outer area of the picture display part, wherein the one corner of the outer area of picture display part is defined between the first gate pad and the first data pad, wherein each of the plurality of the line-on glass signal lines is connected between the first and the second line-on glass signal pads in the one corner of the outer area of the picture display part."

As stated above, none of the cited references, singly or in combination, teaches or suggests at least these features of the claimed invention. Accordingly, Applicant respectfully submits that claim 12 and claims 13-16, which depend therefrom, are allowable over the cited references.

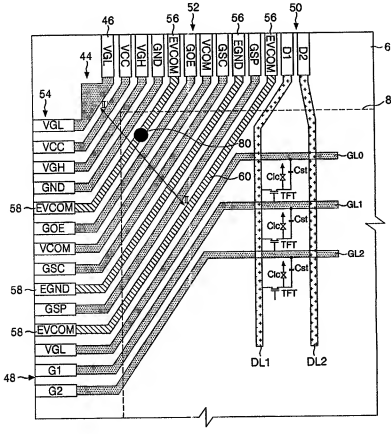
With respect to claim 19, Kawaguchi fails to disclose or suggest a plurality of line-on glass type signal lines located in one corner of the outer area of the picture display part of the lower substrate for applying drive signals to drive the liquid crystal cells, wherein the one corner of the outer area of the picture display part is defined by the intersection of two sides of said outer area of the lower substrate and wherein the gate pad is adjacent to one of the sides and the data pad is adjacent to the intersecting side; a gate insulating layer covering the line-on glass type signal lines; and a plurality of common voltage signal lines for applying a common voltage signal and being formed between line-on glass type signal lines, on the gate insulating layer, wherein at least one of the plurality of common voltage lines applies the common voltage signal through a silver (Ag) dot to a common electrode that is formed on an entire surface of an upper substrate.

Additionally, Song teaches away from being properly combined with the Kawaguchi reference because it deals with applying a voltage to a storage capacitor and to a counter (common) electrode on an upper substrate by connecting one of the storage capacitor electrodes with the counter (common) electrode. The Office Action fails to explain why one of ordinary skill in the art would be properly motivated to turn to this feature of Song to modify Kawaguchi's common electrodes 22/34 which does not have a disclosure of an insulating film on which its common electrodes 23/34 are mounted or a disclosure of a storage capacitor.

Furthermore, Kim fails to disclose a storage capacitor feature that could be commonly fed with a counter electrode.

Because none of the cited references including Kawaguchi, Kim and Song, singly or in combination, teach or suggest the claimed invention, and because the applied references teach away from being combined, as suggested, Applicant respectfully submits that all pending claims under rejection are in condition for allowance.

Applicant also notes that, in the claimed invention, since the common voltage line is the most adjacent to the gate pad and the data pad (please see Fig. 4, as shown below), resistance of common voltage between the gate pad and the data pad can be reduced and delay of common voltage can be reduced. Therefore, deterioration of the image based on a drop of common voltage can be prevented.



In view of the above remarks, it is believed that the present claims under rejection are in condition for allowance and accordingly favorable action is respectfully solicited.

Moreover, Applicant respectfully submits that the withdrawn claims also patentably define over the applied art for reasons similar to those presented above, and respectfully requests that the withdrawn claims be allowed, as well.

New Claims

New claims 24-26 are added. These claims depend from allowable independent claims and further recite a capacitor feature which is neither disclosed nor suggested nor otherwise rendered obvious by any of the applied references.

Consideration and allowance of these claims are respectfully requested.

Conclusion

All of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider all presently outstanding rejections and that they be withdrawn. It is believed that a full and complete response has been made to the outstanding Office Action, and as such, the present application is in condition for allowance.

In view of the above amendment, Applicant believes the pending application is in condition for allowance.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Robert J. Webster, Registration No. 46,472, at the telephone number of the undersigned below to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Director is hereby authorized in this, concurrent, and future replies to charge any fees required during the pendency of the above-identified application or credit any overpayment to Deposit Account No. 02-2448.

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Respectfully submitted,

By DAVID A. BILODEAU USPTO #42,325
Esther H. Chong
Registration No.: 40953
BIRCH, STEWART, KOLASCH & BIRCH, LLP
8110 Gatehouse Road, Suite 100 East
P.O. Box 747
Falls Church, VA 22040-0747
703-205-8000